

Megagate ASICs for the Thuraya Satellite Digital Signal Processor

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Abstract

Boeing Satellite Systems and IBM have designed and fabricated a set of ASIC chip types to perform computation-intensive digital signal processing (DSP) functions on board geosynchronous satellites of the Thuraya mobile communications system. Preparation for this application required comprehensive review of the reliability and space-worthiness of the underlying process and packaging technology. First-pass success on all nine million-plus-gate ASIC designs required extensive model-based simulation and verification. These technologies allowed a four-fold increase in the computational power of the DSP unit over previous systems based on radiation-hardened ASICs, while simultaneously decreasing the number of ASICs required by another factor of five. The first Thuraya satellite is on-orbit, and the whole communications system is performing flawlessly.

1. Introduction

The explosive growth in mobile communications is driving the need for ever-increasing throughput in space-based communications processors. A significant amount of onboard digital signal processing is required to provide the channelization, switching, and user management that enables efficient use of emerging satellite system resources. At the same time, physical and practical limitations on satellite size, weight and power set an upper limit on such processors and ultimately limit the throughput. Similarly, traditional space qualified ASIC technologies lack the speed, density and low power needed for a low risk implementation of complex digital designs. Advanced ASIC technologies are needed to achieve optimum data rates for executing computationally complex signal processing algorithms in the resource-limited space environment.

Advances in deep-submicron CMOS technology, driven by high-volume consumer digital electronics markets, are enabling rapid reductions in ASIC size, weight, power and cost. High density, low power commercial ASIC technologies have the highest potential for meeting space-based communications processor needs, provided that these processes can be adapted to the unique requirements of space. The density of such processes translates to additional capability—specifically, to add channels, increase data rate, enhance routability, increase link margin and add configuration flexibility. At the same time, commercial semiconductor companies have made far larger investments, both in capital equipment and process development, than the traditional suppliers of radiation-hardened ASICs for military and space applications. This investment leads to lower defect density for high volume producibility, and hence, more reliable processes. Satellite DSP system reliability can be improved as a result.

To significantly reduce the mass and size of the satellite electronics, packaging technology needs to keep pace with the quantum leap in CMOS technology. Standard flatpack technology is no longer adequate, due to low input and output pin count and inability to meet electrical performance specifications at high speeds. Megagate ASICs (containing 1 million or more used gates per chip) require advanced area array packages such as Ceramic Column Grid Array (CCGA) or Ceramic Ball Grid Array (CBGA) with flip-chip die attach to reap the full benefit of the semiconductor technology. This next generation of packaging provides significant mass, size and cost improvements over the wirebond multi-chip module (MCM) packaging technology that are the state-of-the-art for radiation-hardened ASICs.

Since 1996, Boeing Satellite Systems (BSS) has been working to make such advanced commercial technologies usable in satellite applications. This effort, called the “Megagate ASIC Initiative” (MAI), has three main components. First, we studied the long-term reliability

and radiation tolerance of commercial semiconductor processes. Second, we studied the space-worthiness of the corresponding advanced packaging technologies. Finally, as these processes offer an order of magnitude more gates per chip than previous radiation-hardened technologies, we worked with ASIC suppliers and CAD tool vendors to develop a compatible design infrastructure and new built-in test methodologies. The most significant payoff of this effort was the adoption of IBM's 0.25 μ m-gate process, 2.5V SA-12 ASIC library and CCGA packaging for the digital signal processor (DSP) in a major communications satellite program.

This DSP is the heart of the Thuraya satellite, a powerful Boeing-built GEO-Mobile (GEM) spacecraft launched in October 2000 for Thuraya Satellite Telecommunications Co., Ltd., based in the United Arab Emirates. Designed by BSS and built by IBM, the nine distinct Thuraya ASICs types contain up to 2.9 million equivalent gates each and represent the first adaptation of commercial ASIC technology to very large-scale digital satellite payloads. Use of commercial technology offered significantly higher density, higher performance, lower power, faster time-to-market and lower cost than the radiation-hardened ASICs used in previous systems.

In this paper we first discuss the approach used to qualify the semiconductor process and packaging technology for space applications, followed by a summary of the design methodology we developed to handle devices of this type and complexity. We follow with a summary of the Thuraya system, the DSP architecture and the design issues specific to the nine ASICs. We conclude with a discussion of the resulting system performance metrics, and a summary of our post-design experience with the ASICs.

1. Process Qualification

Within the Process Qualification task of the MAI, the key objectives were: 1) to identify potentially "radiation-tolerant" semiconductor processes capable of supporting megagate CMOS ASIC chips, and 2) to qualify the most promising of these processes for use in BSS satellite applications. To "qualify" each process, we mean, "to collect data, either from the supplier or by experiment, sufficient to convince both ourselves and our customers that the process is suitable for our applications". This data includes, but is not limited to: 1) reliability of the transistors, metalization and overall product, 2) performance in a radiation environment, including total ionizing dose (TID) effects, single-event latchup (SEL) and single-event upset (SEU) rate, and 3) screening flow required to eliminate any potentially unreliable parts.

Unlike the system described in [1], which required a custom radiation-hardened library on top of the process, a key premise behind the MAI was to use an existing

process and library with little or no modification. This required us to fully understand the degree of radiation-tolerance offered by the existing process and library, and to design around its limitations at the ASIC and unit level. Because commercial suppliers such as IBM neither advertise nor characterize the radiation tolerance of their processes, the burden of radiation effects testing fell to Boeing. Evaluating latchup susceptibility was particularly important because, while there are ways to design around weakness in TID hardness and SEU rate (e.g. adding shielding to reduce TID, or extra circuits to correct soft errors), it is not possible to work with processes that are subject to latchup when hit by cosmic rays.

Because of our long product life and the inability to perform repairs, a very low projected failure rate (both early and average) must be clearly demonstrated. We must demonstrate not only mature semiconductor processes, but also a mature ASIC library, design infrastructure and packaging scheme to go with it.

In the identification phase, we initially considered both suppliers of traditional radiation-hardened ASICs and suppliers of commercial ASICs. It was readily apparent that none of the former was ready to claim "megagate" capability. State-of-the-art commercial processes, deemed unusable earlier, were now considered based on three assumptions, all of which would have to be verified. First, TID radiation effects were expected to reduce in magnitude as gate oxides are made thinner [2]. Second, the capacity and performance of such processes should be sufficient to permit designing around the remaining limitations. Finally, as was mentioned in the introduction, such processes were believed to be at least as reliable as historic "hi-rel" military processes.

IBM was one of a short list of potential commercial ASIC suppliers selected as suitable for committing to a program of radiation testing. The most important criteria used to narrow the list were: 1) feedback on a BSS proposed business model (low volume, high margin), 2) availability of test chips, 3) density, speed and power metrics, 4) latchup susceptibility, 5) reliability data, 6) screening flow, 7) development schedule, 8) CAD tools supported, and 9) types of packaging available. Following this selection, we began to accumulate more extensive data for qualification, including BSS radiation testing.

To mitigate the high cost of radiation testing, the simplest and most critical tests are generally conducted first, and follow-up testing is only done as we continue to see success. A flash X-ray (FXR) test is only a first-order simulation of the cosmic ray induced latchup problem, but it is also the simplest, requiring only supply current to be monitored in-situ. This is followed with cobalt-60 TID testing, which requires parametric characterization before and after irradiation, but no in-situ measurements. Only then do we proceed with a heavy ion SEU rate test, as this requires special test equipment to monitor circuit operation

and count errors in real time. This test also provides verification of SEL immunity in a heavy ion environment.

To develop early confidence in the potential radiation tolerance of IBM CMOS technology, we performed FXR, SEL and TID testing on a 1 Mb SRAM, and TID dose testing on a 0.25 μ m PowerPC microprocessor. The FXR and SEL tests, as well as analysis of holding voltage data provided by IBM, confirmed that the process is latchup-immune (a holding voltage greater than V_{DD} means that a latch condition can not be sustained).

We followed with TID testing of a 2.2 Mgate ASIC test chip used by IBM to qualify the SA-12 library elements, and to verify SA-12 product level reliability. The results confirmed the degree of radiation tolerance seen in the earlier tests, while obtaining data more relevant to chips we would design. The test included evaluation of I/O cells, logic ring oscillators, flip-flops, SRAM and PLL. Similar to other reported studies on deep-submicron CMOS devices [3], the most significant form of parametric degradation in all structures was found to be an increase in standby supply current and I/O leakage current.

We also performed heavy-ion SEU testing of the library test chip. As the device was flip-chip mounted, it was necessary for the SEU test both to choose a facility which could produce especially high energy particles, and to thin the die while mounted in the package, to insure a high penetration of ions to the active devices. Thinning (to less than 100 μ m) was performed by IBM's failure analysis lab. The test was conducted at Texas A&M University's Cyclotron Institute. We measured upset rates for SRAM, register arrays, flip-flops and a PLL macro. The test confirmed that there were no permanent errors created, up to the most energetic particles used.

As expected, the radiation tolerance of the IBM technology fell short of what would be required for it to be considered radiation-hardened (as defined, for example, by government ITAR specifications). Nevertheless, Boeing found the process to be sufficiently radiation-tolerant to be useful in the Thuraya application with appropriate design mitigation techniques.

IBM's philosophy with respect to test and screening, which comes from a long time association with high reliability applications – mainframe computers, was a near-perfect match to BSS requirements. Basic device, metallization and packaging wearout mechanisms are avoided during the product lifetime by obeying a set of design rules built into the ASIC design system, which in turn are based on extensive qualification tests and modeling. The remaining failure rate is determined by the rate at which latent manufacturing defects manifest themselves, and is minimized by tight screens. IBM's "Grade 1" screens (which were developed for mainframe computers) reduce the failure rate target by a factor of 10 over those used for commercial product ("Grade 3") [4]. Part of this screening flow is IBM's "Maverick Control

Process," which eliminates abnormal or low-yielding wafers and lots (a luxury not available to traditional radiation-hardened processes, as the yield is too low, and the volume too low for good statistics). As verified by BSS, the result is a product which exceeds the reliability of lower complexity MIL-STD-883 "Class S" ("space quality") components. With fewer ASICs now required to implement a given function, overall system reliability is improved. The one area where BSS enhanced standard IBM ASIC practice was in I_{DDQ} screening, where we developed a robust statistical analysis method to better spot "out of family" devices within the constraint of limited sample size.

A detailed review of the results from IBM's internal 0.25 μ m process and SA-12 ASIC library certification programs (completed September 1997) was held between BSS and IBM. Finally, a qualification data review meeting was held with the BSS Technical Review Board to go over what had been learned and confirm the process was ready for BSS use. BSS qualification of IBM's SA-12 ASIC technology was completed in June 1998.

2. CCGA Package Qualification

The qualification data review for packages is similar in principle to that for the semiconductor process, but including the following issues unique to space applications: 1) behavior of materials in vacuum and radiation, 2) vibration (low frequency) and shock (high frequency) due to launch and antenna deployment, 3) humidity effects (although there is no moisture in space, corrosion due to pre-launch humidity can cause effects that show up later), 4) thermal coefficient of expansion (a poor TCE match to the board stresses connections) and 5) thermal impedance (without airflow, heat must be extracted from first level packaging by conduction only). Only a subset of the information required is typically available from commercial packaging suppliers, so testing at BSS must augment what the supplier has done.

After extensive literature search and preliminary fatigue analysis, we selected the CCGA packages, concluding that they offer the most reliable product. Data shows CCGA packages have about 10x higher thermal fatigue life than CBGA packages of equivalent size [5]. These CCGA packages employ a high melt solder column connection instead of a solder ball. The columns reduce the effects of CTE mismatches over temperature, improving the integrity of the package column's attachment to the printed wiring board (PWB). The flexible, relatively tall columns provide a reliability that is not attainable with the short solder balls.

We performed mechanical (random vibration and pyroshock) and accelerated temperature cycle (ATC) testing of CCGA technology. Before our testing, little data existed to demonstrate that these packages could meet

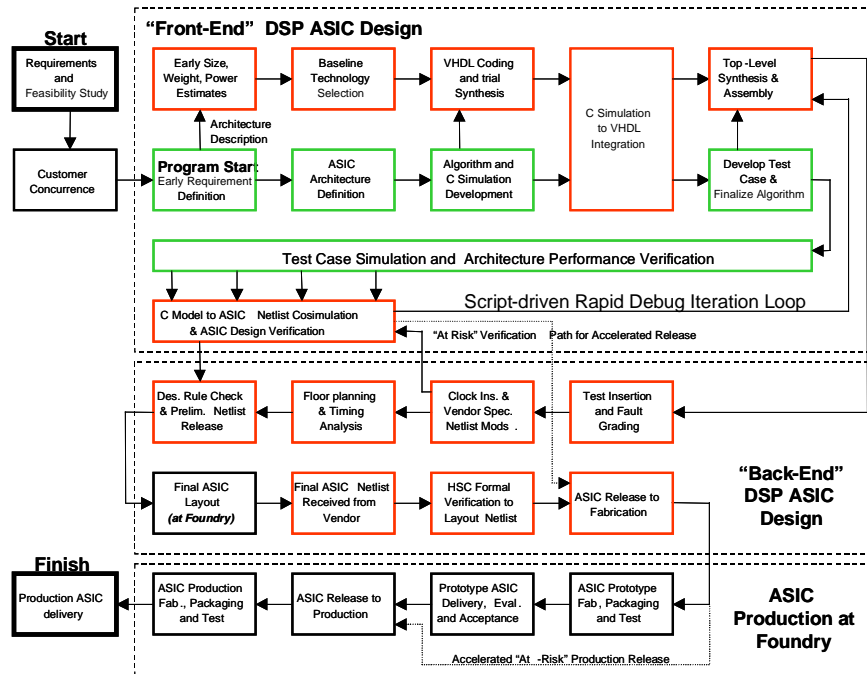


Figure 1. BSS ASIC design methodology.

spacecraft vibration and pyroshock requirements. IBM and BSS designed, fabricated and assembled flight-like PWB test assemblies holding multiple IBM CCGA packages. We exposed the assemblies to levels of vibration and shock far exceeding those expected in the Thuraya mission, demonstrating the robustness of the CCGA packages attached to the PWBs. Based on these tests, we concluded that CCGAs met the Thuraya program’s mechanical margin requirements. ATC “life tests” of several “flight like” slices (two PWBs back-to-back with a heatsink between) also established confidence for CCGA qualification. No abnormalities were observed in any of these tests. At the conclusion of this testing, we constructed a model for thermal cycle fatigue failure rates, applied it to the program’s thermal cycling environment, and concluded that we had sufficient reliability margin.

Using IBM’s CCGA assembly and rework guidelines, a set of robust manufacturing processes was integrated into BSS’s manufacturing flow. Upon review of these processes and the results above, the BSS TRB approved use of CCGAs on Thuraya along with SA-12 ASICs.

3. Design Methodology

An early “pathfinder” SA-12 design was used to refine the design methodology to be used in the flight designs, which were an order of magnitude more complex than those done previously at BSS. Improvements in design entry, verification and analysis were necessary to avoid

unreasonable increases in design cycle time. Within each of these focus areas, we identified particular steps that were candidates for improvement, particularly those known to be labor-intensive, or where significant advances in the supporting tools have occurred. Once we had identified these specific process steps, we conducted research to determine the “best in class” tools for each category. We then evaluated these candidates to determine, first, if they had a good fit into our evolving design process, and second, if they provided the desired productivity enhancement level. All told, we investigated 40 different tools, and down-selected to 18 for detailed evaluations. The resulting design methodology is illustrated in Figure 1.

Front-end ASIC design at BSS utilizes two teams. One team is responsible for the DSP algorithm definition and verification, and the other for the physical implementation of the design in a set of custom ASICs. These teams work in parallel to produce C and VHDL code to validate the system and ASIC’s functional behavior. We extend the system architecture from high-level architecture description to successively lower levels, used to provide requirements to the hardware design team, and to provide the test environment for verifying hardware performance.

We employ a proprietary simulation tool for communication systems, which combines the ability to model end-to-end system performance with the ability to provide stimulus and expected response of DSP processors down to the ASIC partition level. Stimulus/response is clock-for-clock and bit-for-bit accurate, including support for non-DSP auxiliary functions such as configuration and telemetry. System performance evaluation support includes the ability to generate complex user scenarios modeling various link loads and performance factors while gathering data via software spectrum analyzers, bit-error-rate (BER) meters and other measuring and statistical post-processing functions.

This methodology enables exact, automated verification of all DSP ASIC functions directly against system performance criteria without manual comparison of traditional VHDL/gate level simulations against written specifications. All 50 complex ASICs designed at BSS using this cross-verification/simulation approach have worked correctly on the first design pass.

Augmenting workstation compute capability are two hardware accelerators (simulation supercomputers) made by IKOS and Cadence, that are used to vastly speed up simulation of complex ASICs.

With the advent of onboard digital communications processor payloads requiring thousands of ASICs, increasing ASIC complexity and higher packaging density, Design-For-Test (DFT) verticality, integrated from the payload to ASIC wafer levels, becomes essential. Such a capability can significantly reduce processor go/no-go and fault isolation test time at the device, PWB, slice and unit levels. The added structural testing, used in conjunction with the traditional functional DSP testing, improves diagnostic resolution, and reduces failure detection and isolation time at the payload and spacecraft level.

The Thuraya DFT used a combination of IEEE 1149.1 architecture and Build-in-Self-Test (BIST). Both 1149.1 compliant Test-Access-Port (TAP) Controller and National Semiconductor ScanBridge™ macros were embedded in the ASICs. The hierarchical 1149.1 architecture provides both board level testing and unit level backplane and system structure testing. The BIST techniques target logic, memory, process speed, and external mixed-signal design structures (e.g. ADC, DAC).

While DFT had been employed in earlier BSS designs, we refined our design-for-test methodology in three main areas in preparation for design of the Thuraya ASICs. 1) Design of testability macrocell building blocks (TAP, Boundary Cell, Logic/Memory/Interconnect/Analog BIST and Speed Monitor), 2) improved BIST performance (timing, power and area overhead), and 3) automated BIST insertion. The fruits of all of these efforts were validated in the design of the SA-12 pathfinder ASIC.

A key element of the BIST methodology used on the Thuraya ASICs was the LogicVision icBIST™ tool, which provided a highly automated, hierarchical solution for at-speed testing with high fault coverage (> 99% for Logic and 100% for Memory), and supporting test insertion, test bench generation and verification. The ability to self-test using a simple initiation sequence (4K vector set) and short test signature (128 bit), rather than millions of ATPG test vectors, made it easy to employ at all levels of satellite integration in less than 3 ms per ASIC. The ASIC design team solved a key challenge in making commercially available mux-scan and IBM LSSD DFT techniques co-exist. Customized BIST design methodology was mapped into the IBM TestBench and Timing Verification process.

For the Thuraya ASICs, IBM Microelectronics' ASIC group performed the physical design process labeled "back-End" in Figure 1.

4. The Thuraya System

Space-based wireless systems offer a new means of connectivity for a wide audience of users in areas of the

world where telephone lines and other infrastructure for traditional communications are less developed or do not exist. The Thuraya satellite communication system serves the Middle East, North and Central Africa, Europe, the Indian subcontinent and Central Asia with medium-bandwidth data exchange and voice conversations using compact cellular telephone handsets. Thuraya provides over 25,000 simultaneous voice and data communication channels, 25,000 mobile terminal to Public Switching Telephone Network (PSTN) connections, or over 12,500 Mobile to Mobile full-duplex connections. The Thuraya satellites feature a 12.25-meter deployable L-band reflector, on-board digital signal processing with variable-bandwidth channel capability, circuit switching for more than 25,000 full duplex circuits, and agile transmit/receive digital beam forming.

The DSP supports Time-Division Multiple Access (TDMA) mobile terminals and forms 246 (up to 628 are possible) spot transmit and receive beams to support Space Diversity Multiple Access (SDMA). Each beam has programmable channelization and frequency plans within the 34 MHz L Band spectrum. Gateway stations provide PSTN to mobile connections as well as control of the DSP configurations and resources. The Thuraya capacity is 628 total subbands for communications traffic in 4 gateway segments with 160 subbands per gateway segment (156.25 kHz/subband) and 3140 carriers for each of the gateway-to-mobile, mobile-to mobile, and mobile-to-gateway paths (628 subbands × 5 carriers/subband, at 27.7 kHz/carrier). The processor can form a separate beam per subband.

The Thuraya connectivity is from Gateway-to-Mobile and Mobile-to-Gateway with any gateway to any beam and any beam to any gateway, any of 640 gateway subbands routed to any one of the 219 mobile subband frequency slots, and any one of 219 mobile slots to any 628 gateway subbands. Mobile to Mobile connectivity is from any input carrier/time slot to any output carrier/time slot, and any beam to any beam, with 3140 carriers independently selectable per time slot.

5. DSP Architecture

The Thuraya DSP is representative of the class of "distributed real time fixed function digital signal processors" which, by allocating distributed processing elements and memory exactly where it is needed to execute a fixed data flow algorithm, achieve a computational efficiency 10-100 times that of software programmed systems with central computing resources [6]. Although the basic function is fixed, frame formats, channel bandwidth and spacing, filter coefficients and gain distributions have been made configurable in strategic areas of the design to allow reoptimization of processing resources to meet multiple program requirements and to

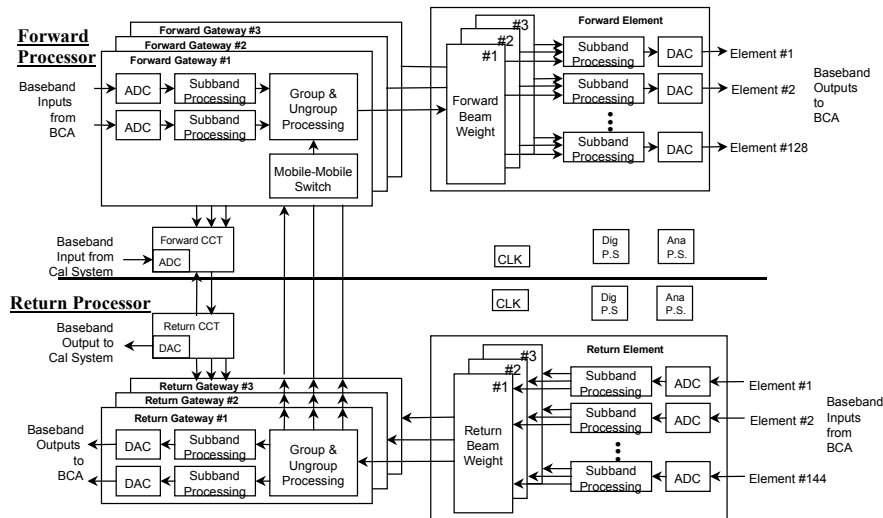


Figure 2. Block diagram of the Thuraya Digital Signal Processor.

adapt to evolving requirements. A block diagram of the DSP unit is shown in Figure 2.

The Thuraya DSP may be thought of as being a set of cooperating kernels which perform certain key functions necessary for the wireless communication task. These kernels include an advanced channelizer which permits us to readily process the time-waveforms received by the wideband N-element sensor-arrays into narrower “subband” segments, a flexible router which permits us to shuffle these narrow sub-bands easily from beam-to-beam, and a precise digital beamformer. The channelizer uses a polyphase filter, followed by a Fast Fourier Transform, to divide the received spectrum into subbands and user channels. The beamformer forms transmit and receive beams by applying complex weights to inputs from and output to elements of a phased array antenna. Using a combination of space, time and frequency diversity, the processor supports up to 25,000 simultaneous user voice channels per satellite. The system is configured completely from the ground, in that the ground system transmits parameters, which determine how the beams are formed, where the sub-bands are routed and how the spectrum is to be divided.

The DSP function is broken into two units. The forward processor processes signals from the C-Band gateway uplink to the L-Band mobile downlink and processes signals for the mobile-to-mobile connection. The return processor handles signals from the L-Band mobile uplink to the C-Band gateway downlink. Both processors consist of gateway and element processing functions. The gateway functions are associated with subband and grouping processing. Subband processing is either dividing an input band of frequencies into smaller subbands or combining subbands into a larger band. The

forward gateways divide bands in subbands, and return gateways combine subbands in bands. Grouping and ungrouping is the process of combining (grouping) or separating (ungrouping) carriers within a subband. The element functions are associated with subband processing and beam forming. Forward elements combine subbands in bands, and return elements divide bands in subbands. Other miscellaneous functions include Command, Control, and Telemetry (CCT), Calibration, Beacon Tracking, clock generation and distribution, and secondary power generation and distribution.

The Thuraya Mobile to Mobile Switch (MMS) is a circuit switch allowing direct connections between users without multiple “hops” between the ground and the geosynchronous satellite. It accepts configuration from the ground network operation control center (NOCC) to setup and/or disconnect mobile to mobile calls. Once the calls have been configured, the MMS switches incoming samples (voice or data samples) at the carrier and time slot level to any outgoing carrier and time slot. Although the MMS is configured for exact Thuraya specifications, it is designed to be extremely customizable, so that it can adapt into various telecom switching standards, including TDMA and GSM, as well as several custom formats, to support a host of other potential customers.

The MMS has been seamlessly integrated with its neighboring digital filters so that it has the ability to compensate for any differences between the ADC sampling rates and the ideal slot and frame times. For instance, if the frame time does not evenly divide into the ADC sampling rate, then the time slots may have fractional ideal samples. The MMS first does a coarse adjustment to the slot switching time at the bit level by keeping track of the number of samples of source and destination slots. Following the coarse adjustment, it takes advantage of its tight integration with the digital filters and changes the filter characteristics dynamically to adjust the group delay in order to provide extremely accurate TDMA slot-to-slot switching times. This feature enhances its ability to be custom tailored to the specifications of various customers.

The MMS implements a completely non-blocking switch. This is partly accomplished by regulating memory access speeds by grouping samples into memory efficient sample groups. Flexibility has been added to be able to

vary the sample group sizes to achieve an integer multiple of sample groups regardless of the configured time slot size or frame size. Implementing such highly configurable sample sorting and manipulation capabilities allows the MMS to optimize memory utilization. The MMS supports multiple TDMA frame sizes simultaneously in the input path as well as in the output path. It also supports different TDMA frame formats and data rate multiples between the input path and the output path. It has the ability to support in-band control signals by injecting control frames periodically between data frames as desired by the customer. The switching logic automatically provides the necessary buffering to compensate for switching between different frame offsets, which can change per output time slot, since different input carriers can be multiplexed on different output time slots on the same output carrier.

6. ASIC Design

Table 1 provides a summary of the nine ASIC types. Complexity of the designs ranges from 830 Kgates to 2.9 Mgates, with 41 to 89% used by memory arrays. Because of the “distributed” nature of the DSP, most of the designs contain many (up to >100) small memory arrays, rather than the few much larger arrays typical of most ASICs. All ASIC I/O and cores run at 80 MHz.

The MMS function is physically implemented in a bit sliced manner using one ASIC type with a larger embedded RAM. Each ASIC switches one bit of every sample in the same manner as other MMS ASICs. The MMS has significant call configuration memory, which is hosted on additional instances of the same ASIC type.

Table 1. Summary of the 9 Thuraya ASICs.

| ASIC Type | Complexity (Mgate) | % Memory | Function |
|-----------|--------------------|----------|---------------------------------------|
| CCT | 1.5 | 49 | Control and data formatting |
| UCC | 2.9 | 62 | Channelization (FFT + FIR filters) |
| GF | 2.9 | 70 | FIR filtering |
| MMS | 2.8 | 87 | Circuit switching |
| GRP | 1.5 | 46 | Channelization (FFT + FIR filters) |
| UGRP | 2.1 | 70 | Channel Assembly (IFFT + FIR filters) |
| DCC | 0.8 | 41 | Channel Assembly (IFFT + FIR filters) |
| RBW | 0.8 | 46 | Digital beam forming |
| FBW | 1.2 | 52 | Digital beam forming |

The Thuraya ASICs were partitioned into “functional blocks,” each less than 200,000 gates in complexity. On previous ASIC designs, we had used a single wireload model for the entire ASIC, which was based on the size of the die. The functional block concept enabled synthesis of the ASICs with a much smaller wireload model, aiding timing closure with tight constraints. All inferred circuitry that was synthesized was required to reside in a functional block; no inferred logic was allowed at the top level of the ASIC. During physical placement of the ASIC,

constrained area regions were used for each functional block partition so that the wireload model used during synthesis would correspond to the physical area used during placement of the functional blocks. Scan chain and BIST macro insertion and verification was similarly done at the functional block level.

The Thuraya ASICs were the first IBM OEM ASIC designs to utilize a new advanced physically-aware electrical and timing correction method. A program called TDCopt (Timing Driven Control Optimization) reads the placed netlist and static timing constraints, and adjusts drive strength, inserts buffers or creates parallel circuits to fix any electrical (capacitance or rise/fall time) rule violations on a net or timing violations for a path. This method reduced design cycle time for the Thuraya ASICs, led to broader use of TDCopt, and ultimately led to the introduction of a further improved IBM tool called PDS (Placement Driven Synthesis).

Due to inserted test logic and redundancy for SEU mitigation, the latency of the clock trees was very large. This caused a large penalty due to Across-Chip Linewidth Variation (ACLV) effects, which were modeled in IBM’s Einstimer™ tool with the Linear Combination of Delay (LCD) method.

In conjunction with IBM, the lower limit of validity for SA-12 timing and electrical models used in the Thuraya ASICs was extended from 2.3V to 2.0V. This allowed an additional degree of freedom to trade power savings for excess timing margin. The nominal supply voltage was reduced from 2.5V to 2.2V, saving 23% in ASIC switching power.

Unlike most ASICs, where minimizing die size is an important constraint, the Thuraya ASICs were deliberately kept larger than otherwise necessary, and logic spread out over the die area. This increased the number of available flip-chip solder-bump connections for heat transfer to the package, and made power dissipation more uniform throughout the chip. A common package design for all 9 ASICs reduced qualification effort and risk.

7. Performance

As there is no central compute resource within the Thuraya DSP, the absolute computational power of the system is not easy to estimate. One instructive approach is to divide the non-memory gate count by the complexity of a standard arithmetic function, and to multiply by the rate at which these elements operate. Using an 8-by-8 fixed-point multiplier as the standard, we estimate the Thuraya DSP has a computational power of over 14 trillion operations per second (TOPS). This is a reasonable approach, because multipliers make up the bulk of the computing logic within the ASICs. Were the same functions implemented in software, we estimate that it would take more than 3000 Pentium III-based computers

to equal the DSP's throughput. To the authors' knowledge, this represents the world's most powerful satellite-based digital signal processor.

A comparison to the previous BSS DSP generation is enlightening. The DSP for ICO, like that for Thuraya, performs channelization, routing and beamforming. For the ICO DSP, we were limited to 0.7 μ m-generation radiation-hardened ASICs, supporting up to 150,000 gates each. In order to achieve reasonable volume and weight at the level of throughput required by system specifications, up to 12 wirebonded ASICs were combined in large (50mm x 100mm) hermetically sealed MCMs. Using the approach above, the computational power of the system is estimated at four TOPS. Each satellite payload required four hardware units (racks), together occupying 0.34 m³ and weighing 270 kg. Total DSP power consumption was over 2000 watts.

The Thuraya ASIC technology from IBM provided improvements of 10x in density, 2x in speed and 2x in power relative to the previous generation used on ICO from traditional military radiation-hardened foundries. This enabled a 4x increase in processing capability, while shrinking size and weight by 30% and maintaining power consumption constant. The collateral benefits were a reduction in ASICs from 2300 to 300, elimination of MCM intermediate packages, reduction from four units to two, reducing design and parts costs by 3x and critical path design schedule by 3 months.

8. Manufacturing and Flight Experience

In a 17-month period, Boeing and IBM designed, built, and delivered nine multi-million-gate ASICs with 100-percent first-pass success, enabling delivery of flight units just 24 months after the official start of design. First-pass success for so many ASICs was unique across the experience of all IBM's ASIC customers, and a testament to the rigorous Boeing design methodology. Just as there were no design errors requiring respin, all nine device types were delivered without fab or assembly related delays. All ASICs met program schedule, quality and radiation requirements with no outstanding issues. This is particularly important, because in the satellite telecommunications industry, a delayed launch could lead to missing a critical market insertion window. The CCGA packaging scheme worked exceptionally well in the BSS manufacturing environment, significantly reducing the rework rate over previous flatpack-style ASICs and MCMs.

On November 12, 2000, Boeing engineers brought the powerful Thuraya digital signal processor online for service, placing phone calls only three days after orbital insertion of the spacecraft at 44 degrees East longitude. Using the satellite's built-in test capability, engineers confirmed perfect performance of this critical commercial

digital signal processing technology in record time. The satellite has since completed on-orbit test and evaluation, allowing Thuraya to begin launching commercial service to more than 20 countries in July 2001. Part of this evaluation has included validation of the cosmic ray induced soft error rates predicted from heavy ion testing.

9. Conclusion

In the Thuraya DSP, Boeing has tapped IBM's advanced custom integrated circuit technologies to improve the performance, reliability and cost of digital satellite-based communications systems. Advancing the state-of-the-art in satellite communications technology has enabled the creation of a viable alternative to land-based communications systems for a wide audience of users. The Boeing GeoMobile product line of regional digital voice and data communications systems is now available on short schedules as space-proven "off-the-shelf" catalog items. A fourth-generation BSS digital signal processor is currently in production for a Boeing 702 Spaceway broadband satellite being built for Hughes Network Systems, scheduled for North American service in 2003. That payload is based on the more advanced IBM 0.16 μ m 1.8V SA-27 ASIC technology with copper metallurgy and with more than 5 million equivalent gates per chip.

10. References

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